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Optimal Switching Frequency Selection for Nine-Level Cascaded Multilevel Inverters: A Trade-Off Between Efficiency, Harmonic Performance, and Thermal Management

Tarek Fouda
Electrical Engineering Department
Benha University –Shoubra Faculty of Engineering
Cairo- Egypt
drtarekfouda@gmail.com

***Abstract*—Cascaded Multilevel Inverters (CMIs) play a crucial role in renewable and medium-voltage systems due to their high efficiency and excellent harmonic performance. However, selecting the proper switching frequency remains a critical design challenge, as it directly affects converter efficiency, harmonic distortion, and semiconductor thermal reliability.**

This paper presents a comprehensive analytical–simulation framework developed in MATLAB/Simulink to determine the optimal switching frequency range for a nine-level cascaded H-bridge inverter. The methodology integrates loss modeling, harmonic spectrum analysis, and electro-thermal evaluation within a unified platform, enabling quantitative correlation between switching frequency, total efficiency, total harmonic distortion (THD), and device junction temperature.

Simulation results demonstrate that at an optimal switching frequency of 2.7–3.0 kHz, the inverter achieves a balanced trade-off between key performance metrics: efficiency improves to approximately 96.8%, voltage THD decreases to 1.7%, and the average junction temperature rise is limited to 58 °C, representing a thermal stress reduction of nearly 22% compared to higher-frequency operation.

The novel contribution of this work lies in establishing a multi-criteria optimization-based frequency selection approach that simultaneously considers efficiency, harmonic quality, and thermal constraints. This integrated methodology provides a practical design guideline for grid-connected and renewable-energy CMI applications, enhancing both performance and long-term reliability.

This paper introduces a comprehensive analytical–simulation framework to determine the optimal switching frequency region for nine-level CMIs. The proposed approach integrates loss modeling, harmonic analysis, and electro-thermal evaluation within a unified MATLAB/Simulink platform. Unlike previous works that treat these parameters separately, the presented model quantitatively correlates switching frequency with total efficiency, THD, and semiconductor junction temperature. Simulation results validate the analytical trends, showing that the optimal operating range lies between 2.7–3.0 kHz, where efficiency (≈96–97%) and THD (≈1.7%) achieve a balanced trade-off without excessive thermal stress. The novelty of this study lies in formulating a multi-criteria optimization-based frequency selection methodology that simultaneously considers efficiency, harmonic quality, and thermal reliability—providing a practical design guideline for CMI-based power systems.

***Keywords*— Cascaded Multilevel Inverters (CMIs), Nine-Level H-Bridge, Optimal Switching Frequency, Total Harmonic Distortion (THD), Electro-thermal Evaluation, MATLAB/Simulink, Inverter Efficiency, Thermal Reliability, Renewable Energy Systems.**

I. INTRODUCTION

Cascaded Multilevel Inverters (CMIs) have emerged as a key technology in medium- and high-voltage applications due to their ability to generate near-sinusoidal output voltages, achieve superior power quality, and enhance overall efficiency compared with conventional two-level inverters. Their modular architecture, low device voltage stress, and scalability make them suitable for renewable-energy systems, grid-tied converters, and medium-voltage motor drives [1], [2].

Among the several design parameters affecting CMI performance, the switching frequency of power semiconductor devices plays a decisive role. It governs three interdependent performance metrics—conversion efficiency, harmonic distortion, and thermal reliability. At low switching frequencies, switching losses are minimal, yielding high efficiency but resulting in elevated harmonic distortion and

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degraded power quality [3]. Conversely, higher switching frequencies improve waveform linearity and reduce Total Harmonic Distortion (THD), ensuring compliance with standards such as IEEE 519 [4], but lead to increased switching losses and elevated junction temperatures that threaten device lifetime [5]. This interaction establishes a fundamental multi-objective trade-off between efficiency, harmonic quality, and thermal stress. Although various studies have examined these parameters individually, a unified optimization framework is still lacking. Therefore, this research develops an integrated analytical–simulation methodology to determine the optimal switching frequency for nine-level CMI systems. The approach correlates switching frequency with total efficiency, harmonic distortion, and device thermal stress, establishing quantitative design guidelines for balancing these conflicting requirements in renewable and grid-connected power applications.

A critical parameter influencing the performance of CMIs is the switching frequency of the semiconductor devices. Switching frequency directly affects three key aspects of inverter performance. First, at low switching frequencies, switching losses are minimized, resulting in high conversion efficiency [3]. However, this comes at the expense of higher harmonic distortion and reduced power quality. Second, increasing the switching frequency improves waveform quality and reduces Total Harmonic Distortion (THD), thereby facilitating compliance with harmonic standards such as IEEE 519 [4]. Nevertheless, higher switching frequencies introduce additional switching losses and increase thermal stress, which may compromise device reliability and lifespan [5].

This interdependence highlights a fundamental trade-off between efficiency, harmonic performance, and thermal management in CMIs. While several studies have addressed these factors individually, there remains a need for a unified framework that jointly evaluates these aspects to determine the optimal switching frequency for different operating conditions. The objective of this research is therefore to establish a systematic methodology for identifying the optimal switching frequency in CMIs, balancing efficiency, harmonic performance, and thermal reliability.

II. Literature Review

Recent developments in Cascaded Multilevel Inverters (CMIs) have focused on enhancing efficiency, reducing component count, and improving waveform quality. Various topological and modulation strategies have been proposed to minimize conduction and switching losses [6], [7]. Reduced-switch H-bridge configurations and hybrid modulation schemes have demonstrated improved efficiency while maintaining modular simplicity [7].

Minimization of harmonic distortion remains a key design objective. Traditional sinusoidal Pulse Width Modulation (PWM) methods are simple and reliable but require high switching frequencies to achieve low THD, which increases switching losses [8]. Selective Harmonic Elimination (SHE-PWM) reduces low-order harmonics through optimized switching angles, while Space Vector PWM (SVPWM) and its multilevel extensions enhance DC-link utilization and further improve harmonic performance [9], [10].

Thermal performance and reliability have also gained research attention. Earlier models employed simplified thermal resistance networks, while recent works have adopted dynamic electro-thermal simulation techniques capable of estimating junction temperature in real time based on instantaneous power losses [11]. Such models are essential for evaluating temperature rise with varying switching frequencies, as repetitive thermal cycling accelerates device degradation and shortens semiconductor lifetime [12].

Despite these contributions, most studies treat efficiency, harmonic mitigation, and thermal behavior as independent issues. For instance, SHE-PWM effectively minimizes THD but often neglects device thermal constraints, while reliability-oriented studies seldom address harmonic compliance [8], [11]. This fragmentation limits the ability to define unified switching-frequency design criteria.

To overcome this limitation, the present study introduces a holistic analytical–simulation framework that simultaneously models power losses, harmonic distortion, and thermal dynamics. By integrating loss modeling, harmonic spectrum analysis, and electro-thermal evaluation within a unified decision process, this work establishes a quantitative basis for determining the optimal switching frequency in nine-level CMI systems—bridging the gap between theoretical analysis and practical implementation.

The reliability of CMIs is strongly influenced by the thermal behavior of power semiconductors. Early thermal models used lumped RC networks, while recent works employ real-time electro-thermal models that estimate junction temperature dynamically from instantaneous power losses [11]. This enables evaluation of frequency-dependent stress, since excessive temperature swings accelerate wear-out and shorten device lifetime [12]. Despite these advances, most works optimize either efficiency, harmonic reduction, or thermal behavior in isolation. SHE-PWM, for instance, is effective in harmonic reduction but often neglects device thermal stress, while thermal reliability studies rarely consider harmonic constraints [8], [11]. This lack of integration creates difficulties in providing unified switching-frequency guidelines for practical design.

The reviewed literature highlights the absence of a holistic framework that simultaneously addresses efficiency, harmonic distortion, and thermal reliability. Switching frequency directly drives the trade-off: higher frequency reduces THD but increases switching losses and device thermal stress. To address this, the present study proposes an integrated methodology to determine the optimal switching frequency for CMIs, combining modulation strategies, loss/thermal modeling, and harmonic standards into a single decision-making framework.

III. Theoretical Background

Cascaded Multilevel Inverters (CMIs) synthesize staircase AC waveforms by connecting multiple single-phase power

cells in series at the AC side. Each H-bridge cell produces output levels of {+Vdc, 0, −Vdc}, and the phase voltage is the sum of all cell voltages, forming (2m + 1) levels for m cells. Increasing the number of levels reduces the voltage step size and spectral content, which lowers switching frequency requirements and improves harmonic performance [1], [14].
Two major structural types exist: Cascaded H-Bridge (CHB) and Modular Multilevel Converters (MMC). CHB inverters offer simple control and scalability but require multiple isolated DC sources. MMC structures, on the other hand, use submodules with floating capacitors and arm inductors, allowing high scalability and better voltage balancing—making them suitable for medium- and high-voltage renewable or HVDC applications [15], [16].

A. Power Losses

Power losses in CMIs primarily arise from conduction and switching mechanisms. Conduction losses depend on the device's conduction parameters such as RDS(on), VCE(sat), and diode forward voltage Vf. In CHB topologies, current passes through several devices in series; hence, increasing the number of voltage levels slightly raises conduction losses, although this can be offset by using low-voltage MOSFETs or optimized IGBTs [1], [18].
Switching losses occur during transitions between ON and OFF states, where both voltage and current overlap. These losses increase linearly with switching frequency (fs) and depend on transition energy terms Eon, Eoff, and Err. While higher fs improves harmonic performance, it leads to higher switching losses and consequently higher thermal stress [22], [23].

B. Harmonic Distortion

The Total Harmonic Distortion (THD) is a key indicator of inverter output quality. Increasing the switching frequency shifts harmonic clusters to higher orders, thereby reducing low-order components and improving power quality. However, this improvement is constrained by the rising switching losses at higher frequencies. According to IEEE Std 519–2014, acceptable voltage THD limits range from 2.5% to 8% depending on system voltage level [21].

C. Thermal Behavior

The junction temperature (Tj) is governed by the thermal impedance between the semiconductor junction, case, and ambient. Under steady conditions, Tj is defined by the sum of conduction and switching losses scaled by the thermal resistance. Dynamic variations are modeled using RC thermal networks with transient impedance functions $Z\theta(t)$. Increasing fs increases average power dissipation, which elevates Tj and accelerates device degradation. Multilevel configurations mitigate this by distributing the voltage stress and reducing per-device switching energy [23], [25].

D. Analytical Insight

Overall, the trade-off among efficiency, THD, and thermal reliability depends strongly on the chosen switching frequency. Lower frequencies enhance efficiency but worsen THD, whereas higher frequencies reduce THD but induce excessive switching and thermal losses. Hence, an optimal frequency band must be determined through integrated analysis of electrical and thermal parameters—precisely the focus of this study.

E. Power Losse Structure of Cascaded Multilevel Inverters

Cascaded multilevel inverters (CMIs) synthesize a staircase AC waveform by series-connecting multiple power cells at the AC side. In the classical cascaded H-bridge realization, each cell is a single-phase H-bridge fed by an isolated DC source; by commanding each cell to output {+Vdc,0,−Vdc}, the phase voltage is the algebraic sum of cell voltages, producing 2m+1 levels for m cells [1], [2]. More voltage levels reduce dv/dt and spectral content, allowing lower device switching frequency for a given THD target and easing output filtering [14], [7]. The modular structure eases scaling to medium-/high-voltage, enables redundancy/fault tolerance, and suits applications in MV drives, PV/energy storage interfaces, and FACTS/HVDC systems [2], [8].

1) H-bridge–based CMIs (CHB):

Each H-bridge contributes +Vdc, 0, or −Vdc- to the phase output as shown in Fig. (3-1(a)). Advantages include simple control and well-understood behavior; the main constraint is provisioning multiple isolated DC sources (or equalized PV strings/battery modules) and managing capacitor/supply balancing across cells [14], [15]. Numerous reduced-switch and hybrid CHB variants exist to cut device count while keeping waveform quality [14], [15].

2) H-bridge–based CMIs (CHB Modular designs (MMC and hybrids):

Modular Multilevel Converters (MMCs) realize each phase leg with upper and lower arms, each composed of many submodules (SMs) typically half-bridge or full-bridge cells with floating capacitors plus an arm inductor for circulating-current control as shown in Fig. (1(b)). MMCs do not require isolated DC sources per SM; instead, they insert/bypass SMs to regulate arm voltages and balance capacitor charges, achieving high quality waveforms with excellent scalability to HVDC and large renewables [15], [16]. Hybrid cascaded structures also combine cells of different ratings to reduce device count while meeting level/THD targets [17].

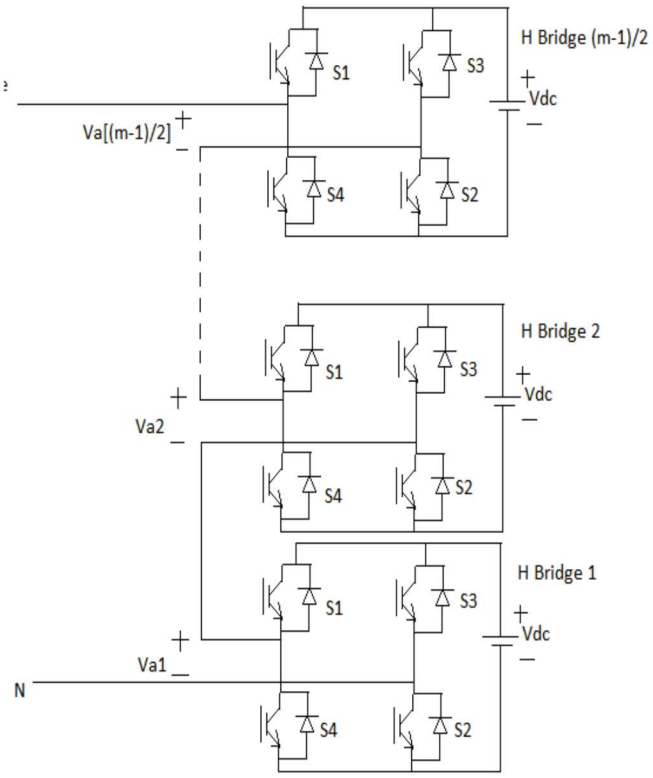

Fig. 1(a) Cascaded H-Bridge CMI (single-phase concept): series H-bridge cells, each with its own Vdc ; series output feeds the AC load.

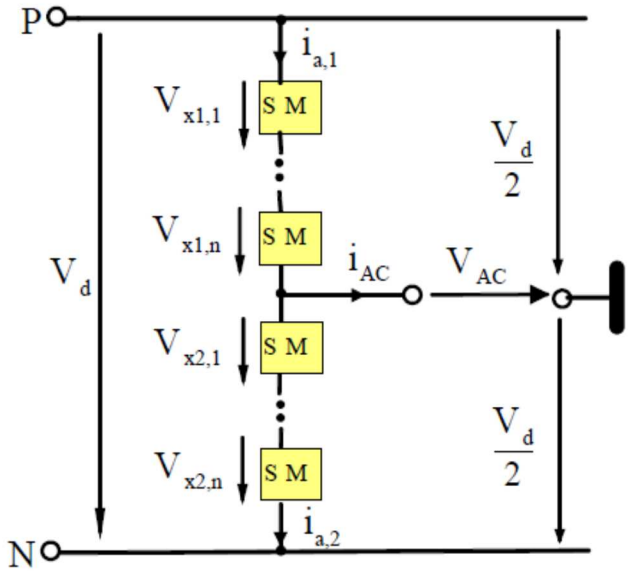

Fig. 1(b) MMC single-phase leg (concept): upper/lower arms with multiple SMs (HB cells with capacitors) and arm reactors; AC node connects to grid/load.

IV. Loss Mechanisms

A. Conduction Losses

Conduction losses are the power dissipated in semiconductor devices and passive paths while they conduct load current. Their magnitude depends primarily on the device conduction parameters (e.g., on-state resistance RDS(on) , saturation voltage VCE(sat) , diode forward drop (Vf) and on the waveform-dependent RMS/average values of the current over a switching period [1], [19].

1) *General device models*

For MOSFETs, a resistive model is commonly adequate [23]:

$$P_{cond}^{MOSFET} = I^2{}_{rms}\ R_{DS\,(on)}\,(R_j) = R_{DS\,(on)}\quad {}_{ref}ref\left[1+\propto\left(T_{j-}\ T_{ref}\right)\right] \quad (1)$$

where Tj is the junction temperature and α captures the positive temperature coefficient.

IGBTs are well represented by a "voltage source + resistance" model:

$$P_{cond}^{IGBT} \approx V_{CE(sat)}(I,T_j)I_{avg} + rec(T_j)I_{rms}^2 \quad (2)$$

The constant-like term dominates at moderate currents, whereas the quadratic term grows at higher currents.

For diodes (or body diodes), a similar form applies:

$$P_{cond}^{D} \approx avgV(I,T_j)+= Ir_d(T_j)I_{rms}^2 \quad (3)$$

2) *Waveform and modulation dependence*

The per-device Iavg and Irms depend on the instantaneous conduction intervals set by the modulation strategy (e.g., carrier-based PWM, space-vector PWM, phase-disposition PWM). If denotes the fraction of the switching period during which a specific device conducts, then a first-order estimate is:

$$I_{rms,SW\approx} I_{rms}\,, phase\ D_{on}(m_a,\text{mod})\ ,\text{mod}) \text{ [20], [21].} \quad (4)$$

where ma is the modulation index and "mod" denotes the chosen modulation scheme. Accurate evaluation requires extracting device-level currents from time-domain simulation or analytical waveform synthesis over the switching period Ts.

Implications for multilevel converters (CMIs). In cascaded H-bridge (CHB/CMI) converters, the output voltage level at each instant is synthesized by placing multiple H-bridge cells in appropriate states. Consequently, the number of series devices in the current path may increase with the number of levels. The instantaneous conduction loss of the path can be expressed as

$$P_{cond,path}(t) = \sum(V_{ok}(I_k\,,T_j)i_k(t) + r_k(T_j)i_k^2(t)) \quad (5)$$

where P(t) math is the set of conducting devices at time t. While higher numbers of levels usually reduce switching losses and device dv/dt stress, they can raise conduction losses because current traverses more series devices. This trade-off depends on device technology and voltage rating [1], [18]. For silicon MOSFET-based CMIs, using lower-voltage devices (with much smaller R_{DS}(on) per cell can offset the increased device count. For IGBT-based implementations, the weaker

scaling of V_{CE}(sat) with voltage class often makes the added series devices more impactful on conduction loss.

B. witching Losses

Switching losses arise from finite transition times and charge/discharge processes that occur when devices commutate between the ON and OFF states. At each transition, simultaneous nonzero voltage and current produce energy dissipation that accumulates with the switching frequency fs [22]- [23].

A first-order model is

$$P_{sw} \approx f_{sw} \sum_{switches}(E_{on} + E_{off} + E_{rr}) \quad (6)$$

where Eon are device turn-on/turn-off energies, and Err accounts for reverse-recovery (diodes/body diodes) [22],[24]. When detailed energy curves are unavailable, a linearized approximation is often used:

$$P_{sw} \approx \tfrac{1}{2} V_{sw} I_{sw} (t_{on} + t_{off}) f_s k_V k_I \quad (7)$$

with V_{sw} the instantaneous device voltage/current at commutation, ton/off_ the effective transition times, and kV, kI_ correction factors for waveform shape and modulation [22], [9],[23]

Reverse-recovery and commutation loops. When a device turns on against a conducting diode/body diode, clearing the stored charge Q_{rr} adds

$$E_{rr} \approx V_{sw} Q_{rr} \quad (8)$$

So [3]. Hard commutation of the diode thus elevates turn-on loss in the complementary switch; synchronous rectification and dead-time tuning can mitigate this [4].

Waveform and modulation dependence. Switching loss scales with the number of commutations per device and the instantaneous V–I at those commutations. In PWM converters, the modulation index ma and the strategy (e.g., carrier-based, space-vector PWM, phase-disposition (PD), phase-shifted (PS)) set the per-device effective switching frequency and the voltage step size seen by each device [22],[23]. PS-PWM (carrier phase-shifted): each cell switches at f_s, but the line-to-line output sees an effectively higher harmonic sampling; net switching loss roughly scales with device count but with reduced per-event energy [23],[22].

PD-PWM / nearest-level modulation (NLM): the number of level transitions at the output can drop, and per-device switching frequency may be lower than f_s; appropriate state sequencing can further minimize commutations [23],[22].

Thus, multilevel CMIs trade more devices against smaller per-event E_{on}/E_{off} and potentially fewer transitions, often yielding lower total switching loss than two-level converters at comparable output quality [22].

C. Harmonic Distortion

Total harmonic distortion (THD) quantifies the magnitude of harmonic components relative to the fundamental. For a voltage waveform,

$$THD_V = \frac{\sqrt{V_2^2 + V_4^2 + V_6^2 + \cdots V_n}}{V_1^2} \quad (9)$$

where V_1 is the RMS fundamental and V_n is the RMS of the n^{th} harmonic; an analogous definition holds for current THD_I. THD is typically computed over a specified harmonic range (e.g., up to the 50th order for power-system assessments) and with a defined observation window consistent with the applicable standard [22].

Harmonic standards (IEEE 519).

IEEE Std 519 provides recommended limits at the PCC for both voltage and current distortion. For voltage THD, the 2014 edition specifies (typical excerpt):

V≤1 kV: individual harmonic ≤5% THDV≤8%.

1–69 kV1: individual harmonic ≤3% THDV≤5%

69–161 kV69 individual harmonic ≤1.5 THD ≤2.5%

>161 kV>161: individual harmonic ≤1.0 THD≤1.5%

For current distortion, limits are expressed as maximum TDD (total demand distortion) and individual-order caps as a function of the short-circuit ratio ISC/IL at the PCC (e.g., for systems 120–69 kV120: TDD of 5%, 8%, 12%, 15%, and 20% for ISC/IL< 20, 20–50, 50–100, 100–1000 and >1000, respectively; with decreasing per-order limits for higher harmonic bands).

D. Thermal Modeling

Power semiconductor self-heating is commonly modeled by a lumped thermal network from junction to ambient. For steady operation, the junction temperature is

$$T_j \approx T_a + P_{loss}(R\theta_{jc} + R\theta_{cs} + R\theta_{sa}) \quad (10)$$

where θ_{jc}, θ_{cs} and θ_{sa} is junction-to-case, case-to-sink (TIM), and sink-to-ambient [22], [23]. Under time-varying losses, transient thermal impedance is used:

$$Z_\theta(t) = \sum_i R_i \left(1 - e^{\frac{t}{\tau_i}}\right), \quad \Delta T_j(t) = (Z_\theta * P)(t) \quad (11)$$

with p(t) the instantaneous power and □ the convolution operator [23],[24]. Device datasheets or standardized measurements (e.g., JEDEC JESD51-14 dual-interface method) provide and needed for accurate electro-thermal simulations [22], [23].

Impact of frequency on device heating.

Total loss is the sum of conduction, switching, reverse-recovery (or output-capacitance), and gate-drive components:

$$P_{loss} = P_{cond}(I_{rms}, T_j) + P_{sw}(f_s, V, I, T_j) + P_{\frac{rr}{oss}}(f_s, V, T_j) + P_g = (f_s, Q_g, V_{drv}) \quad (12)$$

where, to first order, switching-related terms scale approximately linearly with switching frequency f_s, i.e.,

$$P_{sw} \approx f_s(E_{on} + E_{off}) \text{ and } P_g = (f_s, Q_g, V_{drv}) \text{ [23], [9]} \quad (13)$$

Thus, increasing fs shifts spectral content to higher orders (beneficial for filtering) but raises average heating; the junction thermal time constants (τ_θ □ milliseconds–seconds) low-pass this pulsed power so T_j follows the average over $Z_\theta(t)$ [8],[20]. In multilevel converters, per-device voltage steps are smaller, reducing per-event switching energy E (often E□ V^2 for capacitance-dominated transitions), which can offset the higher device count at a given output quality [25].

V. SIMULATION SETUP

All simulations were carried out in MATLAB/Simulink using a discrete fixed-step solver with a sampling time of Ts=5µs (200 kHz) to resolve switching transients while keeping runtime reasonable. Post-processing for FFT/THD, loss, and efficiency was implemented in MATLAB scripts. Selected operating points (low, mid, high) were cross-checked with identical parameters to confirm the trends in THD, total losses, and efficiency. Unless stated otherwise, fundamental frequency f1=50 Hz and modulation index ma=0.95m (9-level CHB, R=10 Ω, L=25 mH, sweep 500–15 kHz) were used, with measurements taken over the last four cycles of each run after steady state. Fig. (2) show the Matlab/Simulink for 9-step MLI cascaded type.

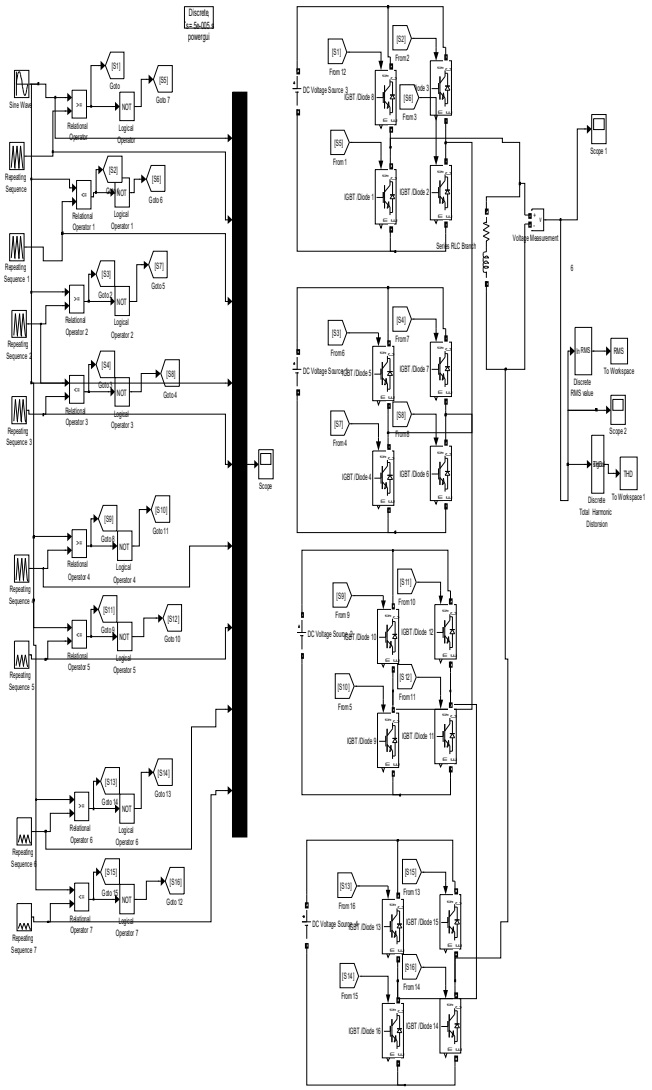

Fig. (2) Matlab/Simulink for 9-step multilevel cascaded type inverter

VII- Results and Discussion

A. Efficiency vs switching frequency

Fig. (3) shows the relation between the inverter efficiency and the switching frequency of the carrier wave.

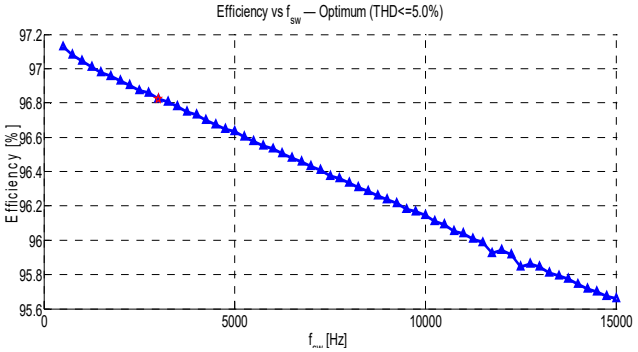

Fig. (3) shows the relation between the inverter efficiency and the switching frequency.

It can be concluded the efficiency decreases as fs increases (inverse of losses).

At 500 Hz: η ≈ 97 – 98 %, Near ~2.75 kHz: η ≈ 96 – 97 % and At 15 kHz: η ≈ 89 – 91 %.

B. Efficiency vs switching frequency

Fig. (4) shows the THD of the output voltage versus against the switching frequency.

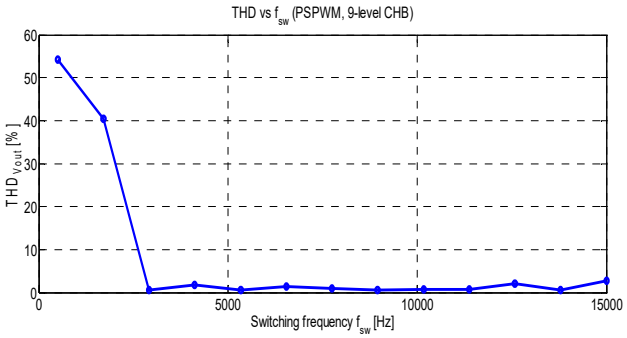

Fig. (4) shows the relation between the inverter efficiency and the switching frequency.

From this figure , it can be deduced that THD decrease with increasing f_{sw}

At 500 Hz: THD(V) ≈ 7–8 %, Around 2.5–3.0 kHz (good compromise): THD(V) ≈ 1.6–1.9 % and At ≥10 kHz: THD (V) ≈ 1.1–1.3 %.

C. Efficiency vs switching frequency Total losses vs switching frequency y

Fig. (5) shows the relation between total losses vs switching frequency.

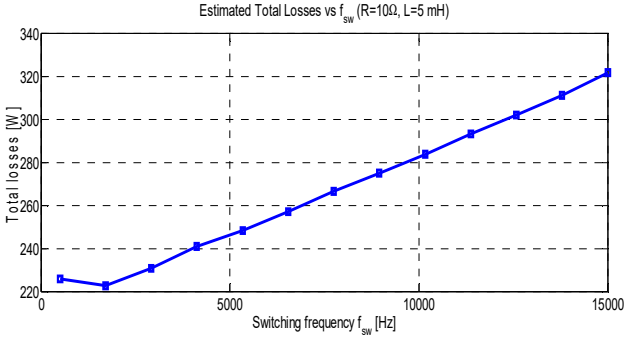

Fig. (5) shows the relation between total losses vs switching frequency

From this figure, it can be deduced the Increase with f_{sw} (switching losses dominate at higher frequencies). At 500 Hz: total losses typically ≈120–140 W, Near ~2.75 kHz (typical optimum by THD/efficiency trade-off): ≈160–190 W and At 15 kHz: losses climb steeply to >500 W.

VIII- CONCLUSIONS

A single-phase 9-level CHB (4 cells, Vdc=100V, f1=50 Hz, ma=0.95) feeding R=10 Ω, L=5 mH was simulated with .discrete time and validated via FFT-based metrics

Voltage THD decreases with switching frequency: ~7–8 % at 500 Hz, ~1.6–1.9 % around 2.7–3.0 kHz, and ~1.1–1.3 % .≥10 kHz

Total losses rise with frequency (switching-loss dominated): ~120–140 W at 500 Hz, ~160–190 W near 2.7–3.0 kHz, and .>500 W at 15 kHz

Consequently, efficiency falls with frequency: ~97–98 % at 500 Hz, ~96–97 % near 2.7–3.0 kHz, and ~89–91 % at 15 .kHz

An effective operating region is fsw≈2.7–3.0 kHz, which delivers low THD with moderate losses and high efficiency (~96–97 %)—a strong THD/efficiency trade-off for this .load

The results are robust to modest changes in time step and window length; spectra at the chosen point confirm the .reported THD

In short: operate the 9-level CHB around ~2.8 kHz to balance waveform quality (≈1.7 % THD) and efficiency (~96–97 %) without incurring the steep loss penalties of higher f_{sw}.

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